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GB 1439351
GB 1301702
DE 2654728A =
GB 1525681
DE 2619664A =
GB 1516058
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(54) Improvements in or relating to a semiconductor device

(57) A semiconductor memory device includes a substrate 18 carrying an epitaxial layer 20 containing an array of memory cells, each cell comprising a single recess 24 in the surface of the device whose lower end penetrates into a buried bit line 16 within the substrate 18. Parallel and spaced apart word lines 14 of conductive material formed on the surface of the device and oriented perpendicular to the buried bit lines 16 extend into the recesses 24 of the memory cells. For each recess 24 a threshold barrier 32 around its upper end, formed by a thick field oxide 30, and a diffusion barrier around its lower end adjacent the buried bit line 16 preferably comprising a region 22 of conductivity value intermediate between those of the substrate 18 and epitaxial layer 20, combine to define a charge storage area in the material forming the walls of the recess, so that the portion of a word line within each recess provides a gate for modulating the flow of charge to and from the bit line during read and write operations.

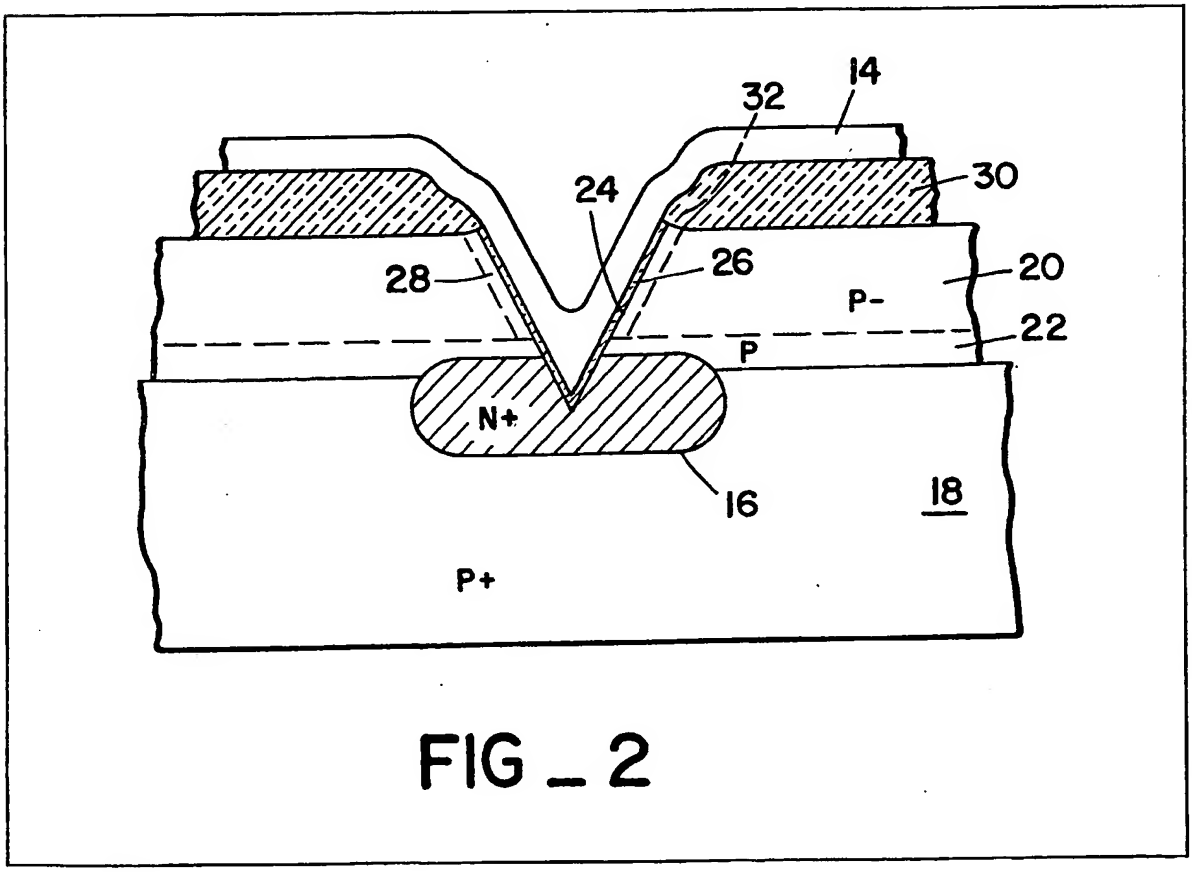

FIG_2

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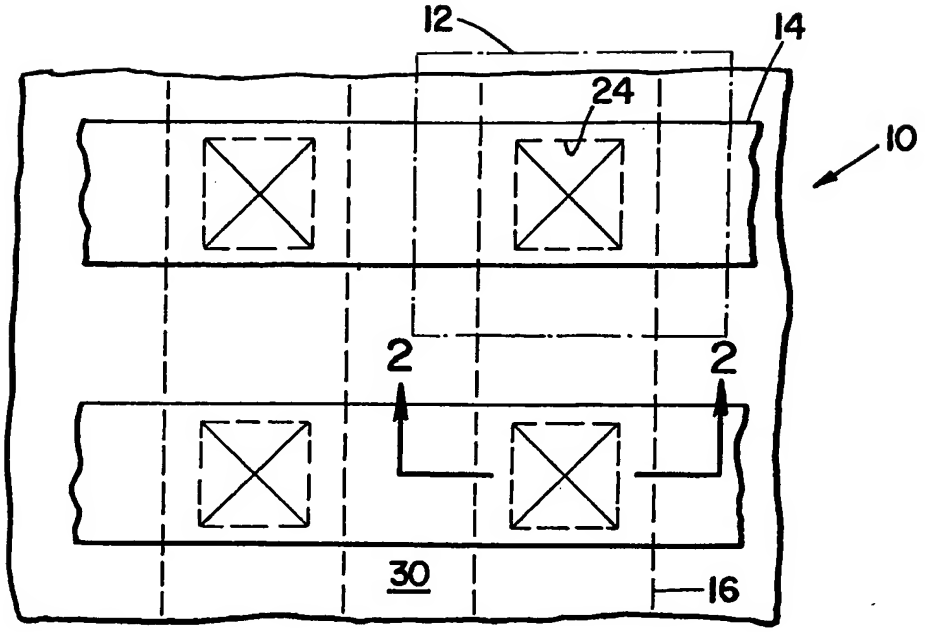

FIG_1

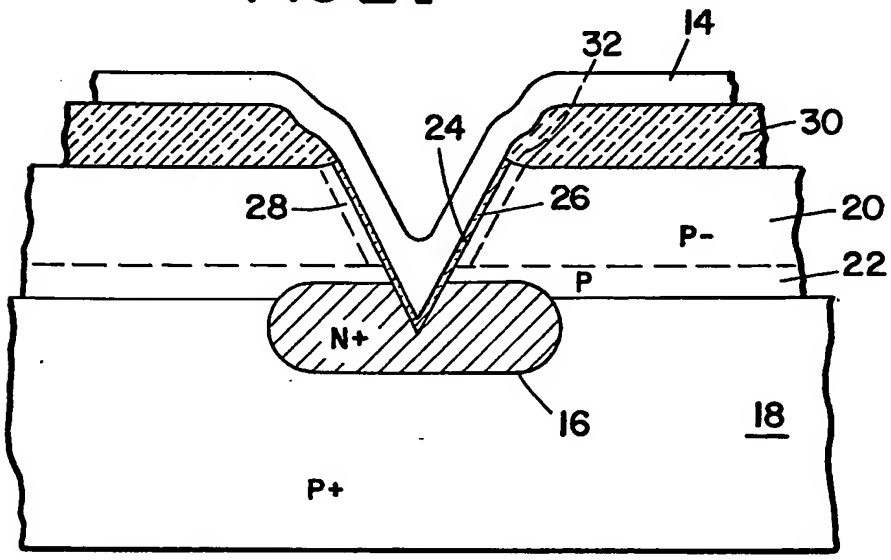

FIG_2

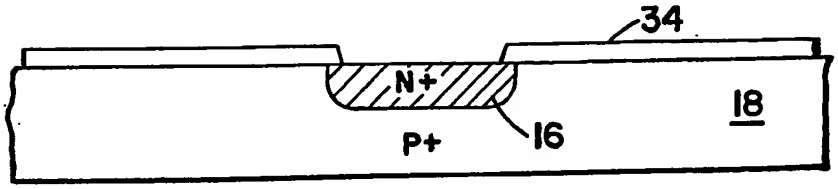

FIG_3a

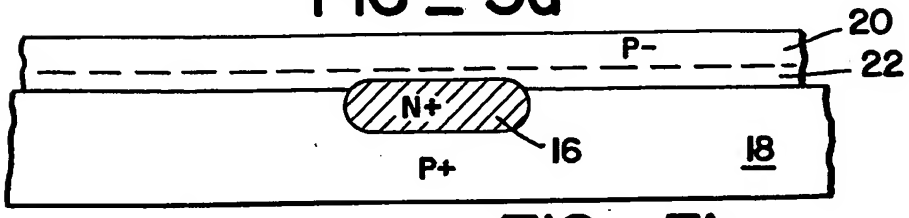

FIG_3b

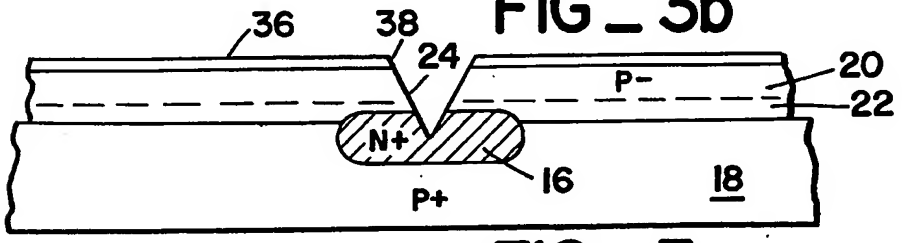

FIG_3c

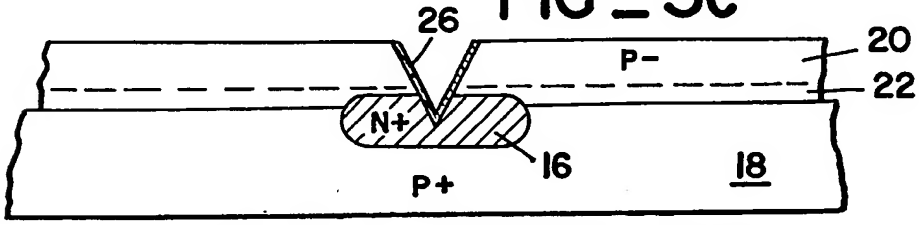

FIG_3d

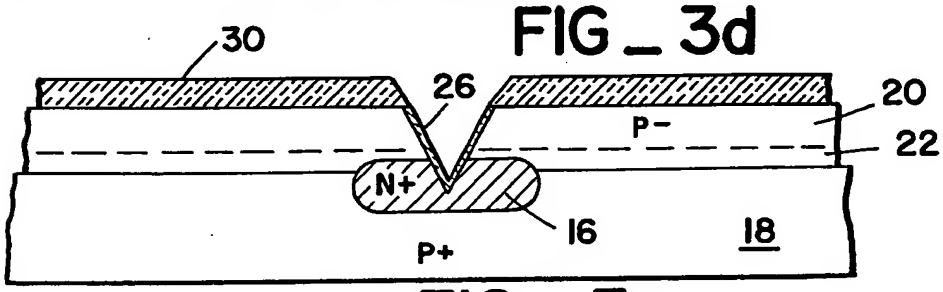

FIG_3e

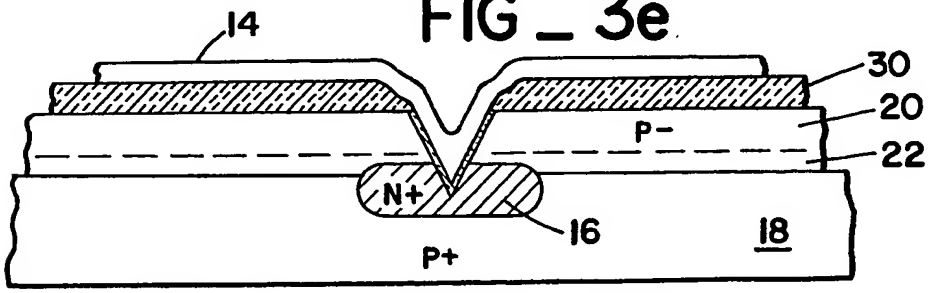

FIG_3f

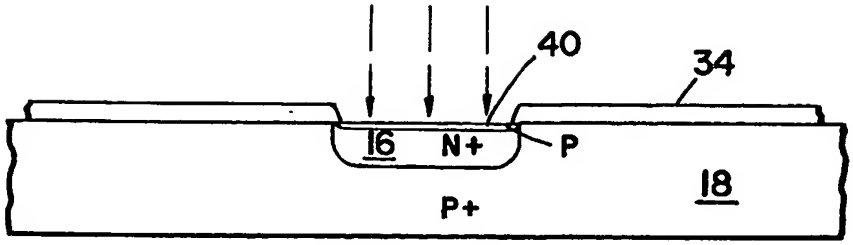

FIG_4a

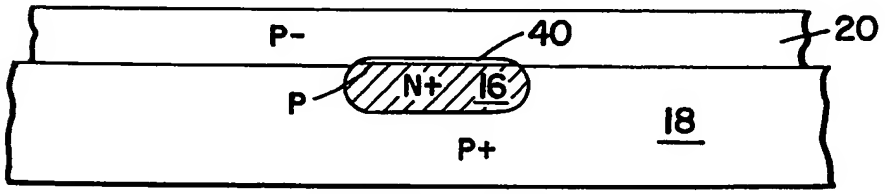

FIG_4b

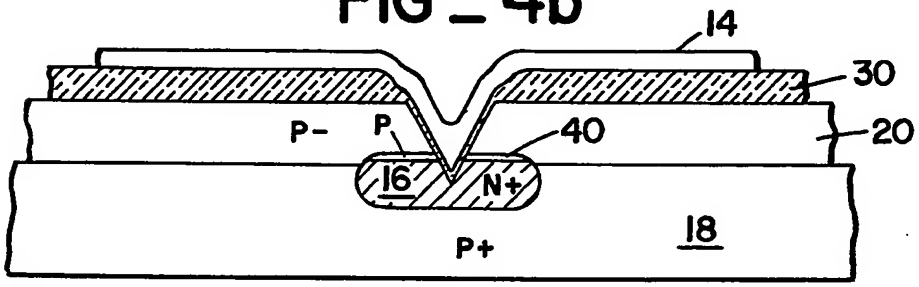

FIG_4c

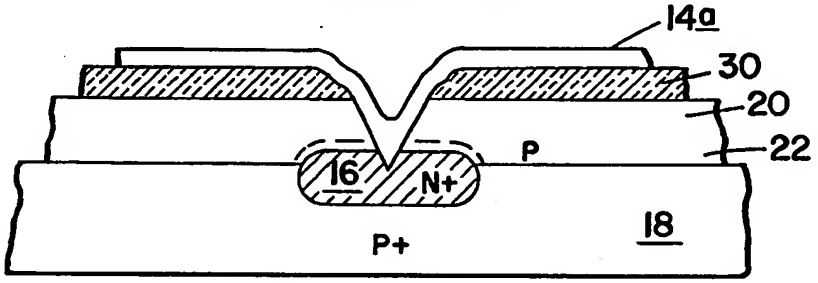

FIG_5

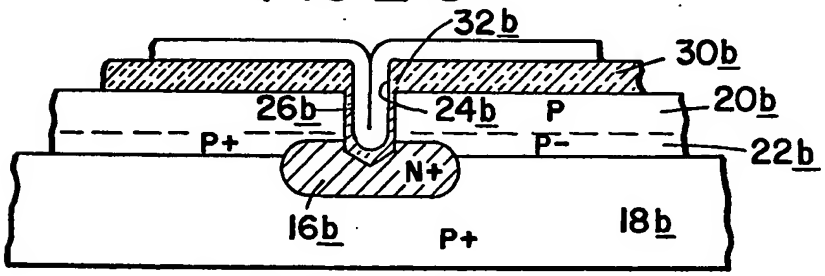

FIG_6

SPECIFICATION

Improvements in or relating to a semiconductor device

THIS INVENTION relates to semiconductor logic or memory devices and to a method for making same.

In U.K. Patent Application No. 20567/76 (Serial No. 1531824) corresponding to U.S.A. Patent Specification No, 4,003,036 a single IGFET memory cell with a buried storage element is disclosed for use in a semiconductor read-write memory device. Briefly, this prior art memory cell utilized a buried storage element of a first conductivity type (N +) located within a substrate of another conductivity type (P +) material. An etched recess having a V-shaped cross-section had a lower end that extended into the buried element which formed the source of a VMOS transistor. The recess also extended through another region of the first conductivity type material that formed the drain of the VMOS transistor near its upper end. The recess walls were provided with a thin gate oxide material and this oxide was covered by a conductive material serving both as a gate and also forming a portion of a word line for the device. In operation, the buried N + source element formed the storage device for the cell and the drain region formed a portion of buried bit lines. The aforesaid prior art single transistor cell provided an improvement in the art with significant advantages over previously developed three transistor and six transistor planar type memory cells. However, it also required the formation of transistor drain regions and the charge capacity of the device was limited by the size of the buried N + storage element.

According to this invention there is provided semiconductor memory device comprising a substrate of a first conductivity type material; a plurality of elongated regions of a second conductivity type material within said substrate forming bit lines; an epitaxial layer of lightly doped first conductivity type material covering said substrate and said elongated regions; a series of recesses extending from the surface of said epitaxial layer and spaced apart along said elongated regions, each said recess being formed by sidewalls that extend into a said elongated region; a relatively thick field oxide layer extending over said epitaxial layer and surrounding each said recess, said thick oxide forming a field threshold barrier around the upper end of each of said recess; a series of parallel, spaced apart and elongated regions of conductive material forming word lines on said field oxide layer, each said word line extending transversely to said buried bit lines and between a series of recesses; means on or adjacent said elongated bit lines near the lower end of each said recess forming a diffusion barrier; and charge storage regions formed in the side walls of each said recess between its said diffusion barrier and said field threshold barrier.

A presently preferred embodiment of a memory device according to the present invention comprises one having an array of cells wherein each cell comprises an etched recess having a V or U-shaped cross-section extending into the upper surface of a semiconductor substrate. The substrate, or a first conductivity type, has a plurality of buried bit lines of an opposite conductivity type and the lower end of each recess extends into one bit line. Surrounding the lower end of each recess adjacent to and above the buried bit line is a diffusion barrier for preventing the leakage of charge from the remaining area around the sides of the recess. Within the recess its sides must be covered with a thin gate-oxide layer in an IGFET type structure. Alternatively, the walls of the recess could be covered directly with a conductive material which forms a junction field effect transistor (JFET)-like device. For the IGFET device, the oxide is covered with a conductive material that may be metal or poly-crystalline silicon. This conductive material (for either case) forms a gate for the memory cell and also forms a portion of an "X" line or word line that runs transversely to the buried bit line or "Y" line. When used in a semiconductor device comprised of a large number of word lines and buried bit lines a memory cell may be formed at each intersection or crossover of these lines. In effect, the area forming the walls surrounding each V or U-shaped recess becomes a relatively large charge storage region for the cell and the charge is kept within this area by an isolating threshold barrier near the top and the diffusion barrier near the bottom of each recess.

In use, when it is desired to write into the cell, a voltage is applied to the buried bit line and thereafter another voltage is applied to the word line, the latter voltage being of such a nature that it will lower the surface potential on the recess walls. This causes a thin layer of epitaxial material around the recess walls to function as a storage element and attain a surface potential equal to that of the bit line below. When the surface potential on the word line is removed, the diffusion barrier between the buried bit line and the charge storage region is now cut off so that the charge storage region in the walls of the recesss is isolated and separate. This charge remains in storage until such time as the cell is read. To sense the charge or read the cell a voltage of the proper polarity is once again placed on the word line and causes an electrical connection between the charge storage region and the bit line through the diffusion barrier. Thus, a certain amount of charge determined by surface potentials and geomet-

ric factors is transferred to the bit lines which causes a certain potential differential between the existing level and the original bit line level, which may be sensed by a differential amplifier.

In order that the invention may be more readily understood, and so that further features thereof may be appreciated, the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a schematic plan view of a portion of a semiconductor memory device utilizing charge storage cells according to the present invention;

Figure 2 is a view in cross-section of one memory cell in accordance with the present invention taken on the line 2–2 of Fig. 1;

Figures 3a–3f are a series of views in cross-section showing the method steps for constructing a memory cell according to the invention;

Figures 4a–4c are a series of views in cross-section showing some alternate method steps for forming the lower diffusion barrier region according to the invention;

Figure 5 is a view in vertical cross-section of a modified form of memory cell according to the invention; and

Figure 6 is a view in vertical cross-section showing another alternate form of memory cell in accordance with the present invention and utilizing a U-shaped recess.

Referring to the drawing, Fig. 1 shows a schematic plan view of a semiconductor memory device 10 in accordance with the present invention. The portion of the device illustrated comprises an array of memory cells 12 formed at the intersections of parallel word lines 14 and a series of buried parallel bit lines 16 oriented in a direction 90° to the word lines. Thus, in the array, the memory cells are closely packed because the parallel word lines and parallel bit lines are located relatively close together, using conventional semiconductor design rules, and each memory cell requires substantially only the area formed by a word line and bit line intersection or crossover.

In Fig. 2, the structure of a typical single memory cell 12 according to the invention is shown in vertical cross-section. The entire memory device is formed as an integrated circuit on a base semiconductor substrate 18 of P or N material. In the embodiment illustrated, the base substrate is crystalline silicon material having a generally uniform thickness (e.g. 250 microns). This material is provided with a P+ type conductivity by doping it with boron to a level of around 10^{15} to 10^{19} atoms per cubic centimeter.

The parallel bit lines 16, having a substantially uniform width and spacing are formed of regions of N+ material within the base substrate 18. The thickness of these bit lines is substantially uniform (e.g. around 2 microns) and the N+ type conductivity, preferably with a concentration of around 10^{19} to -10^{20} atoms per cubic centimeter, may be provided using a dopant with a small diffusion coefficient, such as arsenic or antimony.

Covering the base substrate 18 and the bured bit lines 16 is an epitaxial layer 20 of lightly doped P or P− material formed by a standard chemical vapour deposition (CVD) type of process. Along the interface of this layer 20 and the base substrate 18 is an intermediate layer 22, also of P material, but more heavily doped P material than the epitaxial layer 20.

Extending downwardly from the surface of the epitaxial layer 20.

Extending downwardly from the surface of the epitaxial layer 20 at each cross-over area of a word line and a bit line is an inverted pyramid-shaped recess 24 having a V-shape in its vertical cross-section. These recesses 24 are formed by an anisotropic etching process which has a low rate of attack along (111) planes and a high attack rate on (100) planes, as described in U.K. Patent Specification No. 1,488,151. This etching process thus forms recesses 24 with downwardly converging side walls, and the lower apex of each recess formed by its converging side walls extends into a buried bit line 16. The horizontal cross-section of each recess 24 has a square or rectangular shape. All of the sloping walls of each recess 24 are covered with a thin gate oxide layer 26 of silicon dioxide which also extends below the upper surface of the exposed buried bit line 16. The word lines 14 are formed of a conductive material such as a suitable metal or polycrystalline silicon and each recess is partially or substantially filled with such conductive material.

The epitaxial lightly doped P-material 20 forming the sloping sidewalls of each V-shaped recess 24 comprise a charge storage region 28 that extends completely around the recess adjacent to the thin gate oxide layer 26. As indicated by the dotted line in Fig. 2, this charge storage region 28 may have a shallow depth, (measured in a substantially horizontal direction as shown in Fig. 2) but its charge capacity is relatively large since it covers the area of all four sloping walls of each recess.

The upper edges of the gate oxide layer 26 terminate around the edges of each V-shaped recess and at this point the thickness of the oxide increases abruptly to form a relatively thick insulative oxide layer 30 that covers the epitaxial layer 20 at least around the various recesses 24. This relatively thick oxide layer 30 forms a barrier (indicated by the numeral 32) around the upper end of each recess to help retain charge concentration within the sloped charge storage region 28. This retention of charge is based upon the effective

surface potential under the thick insulator region 30 for the voltages used during the operation of the cell.

Surrounding the lower end of each recess the relatively higher P doped intermediate layer 22 (as compared with the epitaxial P-material) forms a lower barrier for the charge storage area. These upper and lower barriers serve to retain the charge concentration of electrons within the storage regions 28 formed in the sloped side walls of each recess. In accordance with well-known principles of field effect devices, the layers 22 and 30 are effective as barriers because of the quasi Fermi level in the silicon which prevent the electrons from moving away from the walls of each recess, either along the top surface 30 or into the top surface of the buried bit layer 16 at the bottom of the recess.

In addition to its barrier function the intermediate P layer 22 serves as a transfer region that helps to control the flow of electrons from the bit line into and out of the charge storage region 28. Moreover, this transfer region or diffusion barrier 22 is modulated by the gate portion of the word line covering the gate oxide layer within the recess.

In the operation of a memory cell 12 according to the invention, when it is desired to write into the cell a voltage is first applied to the appropriate bit line. Thereafter, a voltage is applied to the word line of such a nature that it will actually physically lower the surface potential of the transfer region. That is, the positive voltage on the word line (and thus on the gate of the cell) acts in essence to turn on the transfer region between the bit line and the charge region 28. When this occurs, the charge storage region will attain a surface potential equal to that of the bit line and thus the charge becomes stored there. Now, the surface potential in this charge storage region is controlled by the bit line 16. When the voltage or surface potential on the word line is removed, the flow of electrons between the bit line and the charge storage region ceases. At this point, the surface potential is isolated within this storage region. Since the charge storage regions 28 extends completely around the recess on all of the sloping walls, it thus covers a relatively large area, and accordingly its charge capacity is also relatively high. Thus, when this write procedure is complete, a strong, durable signal is stored in or locked into the memory cell.

When it is desired to sense the stored charge in a "read" mode for the cell, to determine whether a "1" or an "0" is present therein, the function of the elements is similar. At this point, the bit line is "floating" or at some intermediate potential that is predetermined and from which all relative changes will be made. A positive value voltage is applied to the word line which again causes the bit line to connect with the charge storage region 28. This causes the circuit to come to equilibrium with some potential differential from its original potential occurring on the bit line, which charge is detectable by a suitable differential sense circuit on the device. Such a sense amplifier circuit is well-known in the art of memory devices and therefore will not be described here in detail.

The aforesaid write and read functions of the memory cell 12 can be expressed mathematically by applying the rules of conservation of surface potential during the write-in phase and the conservation of charge during the read-out phase and then the sensing of differential voltage in reading.

One method for producing a memory device in accordance with the present invention will be described with reference to Figs. 3*a* to 3*f*. A substrate 18 of crystalline silicon material having a P + type conductivity concentration of 10^{15} to 10^{19} atoms/cc is provided. The substrate has a crystallographic orientation with the (100) plane at its surface so that V-type grooves or recesses can be formed therein by an anisotropic etchant.

To form a first mask, the substrate 18 is provided with a layer 34 of silicon dioxide which may be formed by oxidizing the substrate surface in steam at 800°–1,200°C. The oxide layer is then treated with a suitable etchant (e.g. buffered hydrofluoric acid) to remove the oxide at the areas on the substrate surface where the buried bit lines 16 are to be formed. As shown in Fig. 3*a*, a diffusion of N^+ material (e.g. antimony) into the substrate is now performed to form a buried N + layer 16 having a thickness of around 2 microns. The oxide layer 34 is then removed leaving the substrate with a series of parallel N + strips with the desired spacing on the substrate.

In the next step of the method, as shown in Fig. 3*b*, an epitaxial layer 20 of lightly doped P-material is formed on the substrate surface and over the N + regions 16. This layer can be formed by the thermal decomposition of silane (SiH_4) at a temperature of around 800°–1,000°C. in an epitaxial reactor to a thickness of around 2.5 microns. During the application of this epitaxial layer 20, including the siluntaneous heat treatment, an out-diffusion of P material from the P type substrate occurs which forms the interface barrier layer 22 that extends for about 0.5 microns above the N + buried layer. A similar out diffusion at the N + dopant, e.g. the antimony, also causes the N + region to extend slightly into the epitoxial layer 20.

Now, another oxide layer 36 is applied over the device and a second mask is used to define spaced apart openings 38 directly above and in line with the buried N + regions. Using an anistotropic etchant (e.g. hydrazine and water) a V-type recess 24 is

formed in the device at every opening above an N + region, the bottom of each recess penetrating into the buried N + region, as shown in Fig. 3*c*.

Using a conventional oxidation procedure, a thin gate oxide 26 with a thickness typically 500Å to 1000Å is now grown with each recess 24. This stage is illustrated in Fig. 3*d*.

Now the V-groove recess areas are masked, as further oxidation is accomplished to provide the field oxide layer 30 surrounding each recess. This is the stage illustrated in Fig. 3*e*.

Thereafter, another mask (not shown) is utilized to form the conductive word lines 14 as shown in Fig. 3*f* that extend from recess to recess and perpendicular in orientation to the buried bit lines 16. The word lines may be polycrystalline silicon or metal and covering them may be a suitable passivation layer (not shown) of some effective insulative and protective material.

Contacts (not shown) may be provided from the surface of the device by vias through the epitaxial layer 20 to the various bit lines where necessary, and in accordance with well-known design principles.

As previously described, the interface layer 22 of P material provides the diffusion barrier for the charge region 28. Other forms of this diffusion barrier may be provided within the scope of the present invention utilizing some other different method steps. For example, as shown in Figs. 4*a* to 4*c*, the diffusion barrier may be formed by the diffusion or ion implantation of a thin P layer 40 directly on the N + regions.

This extra diffusion or ion implantation step would be performed just after the N + regions are formed using the same mask 34 and before the epitaxial layer 20 is grown thereon, as shown in Fig. 4*a*. Thereafter, the epitaxial layer 20 may be applied as previously described. This is the stage shown in Fig. 4*b*. When the V-shaped recesses are formed, the P layer 40 on each N + bit line 16 surrounds the lower portion of each recess thereby performing its barrier functtion. This is the stage shown in Fig. 4*c*.

Another form of diffusion barrier may be formed by providing a layer of P material on all areas of the substrate other than the N^+ regions. This procedure, however, requires the application of an additional mask after the N^+ regions have been formed. Subsequent heat treatment will cause the P material to diffuse over the N + regions surrounding each recess, thereby forming another form of lower diffusion barrier.

In an alternate form of the invention the insulated gate field effect transistor (IGFET) embodiment, just described, may be replaced by a junction field effect transistor (JFET) arrangement. In this latter embodiment, as illustrated in Fig. 5, no thin oxide layer is provided within the recess for the cell. Instead, a suitable conductive material 14*a*, such as platinum or some other metal is used for the word lines. Within each recess the metal is applied directly to the recess walls and provides a Schottky effect to transmit charge carriers. Here the function of the upper and lower barriers and the surrounding charge storage regions is exactly the same as with the previously described IGFET version.

Although the invention has been described in terms of embodiments wherein said recesses formed by an isotropic etching are V-shaped in cross-section, it may also be embodied in a semiconductor device 10*b* as shown in Fig. 6 wherein recesses 24*b* are formed having U-shaped cross-section with parallel, rather than downwardly converging side walls. Such recesses are formed when the silicon wafer is first cut with its horizontal surface in the (110) crystalline plane and its (111) planes perpendicular to the horizontal plane. As shown in Fig. 6, the U-shaped recess 24*b*, like the previous V-shaped recess 24 extends through an epitaxial layer 20*b* and into a bit line 16*b* formed within a substrate 18*b*. The device may have a thin oxide layer 26*b* within the recess as shown in the IGFET version or it may have the Schottky type JFET construction similar to that shown in Fig. 5. Within the U-shaped recess is a layer of conductive material 14*b*, such as polycrystalline silicon which provides a gate portion of a word line. In the same manner as the V-shaped cell embodiment, an upper charge barrier 32*b* is formed around the open end of each recess by a relatively thick insulating oxide layer 30*b*. Also, a lower charge barrier is formed by a thin P layer 22*b* that covers the buried bit line region 16*b* around the lower end of each recess. These upper and lower barriers control the charge storage region in the parallel side walls of the recess 24*b* in the same manner as with the V-shaped recesses 24, previously described.

CLAIMS

1. A semiconductor memory device comprising: a substrate of a first conductivity type material; a plurality of elongated regions of a second conductivity type material within said substrate forming bit lines; an epitaxial layer of lightly doped first conductivity type material covering said substrate and said elongated regions; a series of recesses extending from the surface of said epitaxial layer and spaced apart along said elongated regions, each said recess being formed by sidewalls that extend into a said elongated region; a relatively thick field oxide layer extending over said epitaxial layer and surrounding each said recess, said thick oxide layer forming a field threshold barrier around the upper end of each said recess; a series of parallel, spaced apart and elongated regions of conductive material forming word lines on said field oxide layer, each

said word line extending transversely to said buried bit lines and between a series of recesses; means on or adjacent said elongated bit lines near the lower end of each said recess forming a diffusion barrier; and charge storage regions formed in the side walls of each said recess between its said diffusion barrier and said field threshold barrier.

2. A memory device according to claim 1 wherein said substrate is P + type conductivity silicon material, said bit lines have an N + type conductivity and said means forming a diffusion barrier is an intermediate layer of P material covering said bit lines around the lower end of each said recess.

3. A memory device according to claim 2 wherein said epitaxial layer is P − type material that is more lightly doped than said intermediate layer.

4. A memory device according to any one of the preceding claims wherein said substrate material with its epitaxial layer has an upper surface in a (100) crystal plane and each said recess in said upper surface has a V-shaped cross section.

5. A memory device according to any one of claims 1 to 3 wherein said substrate material has an upper surface in a (110) crystal plane and each said recess has parallel side walls with a bottom forming a U-shaped cross section.

6. A memory device according to any one of the preceding claims including a relatively thin oxide layer covering said sidewalls of each said recess, said conductive material of one of said word line covering said thin oxide layer within each said recess.

7. A memory device according to any one of the preceding claims wherein said conductive material of said word lines is polycrystalline silicon.

8. A memory device according to any one of claims 1 to 6 wherein said conductive material of said word lines is metal covering the wall surfaces of each said recess and producing a Schottky effect for transmitting charge between said charge storage regions and said bit lines.

9. A method for manufacturing a semiconductor memory device including the steps of providing a substrate of crystalline silicon material having P + type conductivity; forming a series of spaced apart diffused strips of N + type conductivity material within said substrate to provide buried bit lines; forming a diffusion barrier layer over said buried bit lines of P type material that is less heavily P doped than said substrate; forming an epitaxial layer on said substrate having a lightly doped P − type conductivity that is less heavily doped than said diffusion carrier layer; etching a plurality of spaced apart recesses within the surface of said device which are aligned so that each recess extends through said epitaxial layer into a said bit line; forming a relatively thick layer of oxide material around the upper edges of said recesses; and forming a series of conductive lines of conductive material on said oxide material which are transverse to said buried bit lines, each said word line interconnecting an aligned series of said recesses and covering the sidewalls of each aligned recess.

10. A method according to Claim 9 wherein the step of forming said diffusion barrier comprises heat treating said device during the application of said epitaxial layer to cause an out-diffusion of P material into said epitaxial layer.

11. A method according to claim 9 wherein the step of forming said diffusion barrier comprises diffusing by ion implantation a thin layer of P dopant material into said diffused strips of N + material immediately after forming them and by utilization of the same mask.

12. A method according to any one of claims 9 to 11 including the step of forming a thin layer of gate oxide material within each said recess before forming said conductive word lines within said recess.

13. A semiconductor memory device substantially as herein described with reference to and as shown in Figs. 1 to 3 of the accompanying drawings.

14. A semiconductor memory device substantially as herein described with reference to and as shown in Fig. 4 of the accompanying drawings.

15. A semiconductor memory device substantially as herein described with reference to and as shown in Fig. 5 of the accompanying drawings.

16. A semiconductor memory device substantially as herein described with reference to and as shown in Fig. 6 of the accompanying drawings.

17. A method of making a semiconductor memory device substantially as herein described with reference to Figs. 1 to 3 of the accompanying drawings.

18. A method of making a semiconductor memory device substantially as herein described with reference to Fig. 4 of the accompanying drawings.

19. Any novel feature or combination of features described herein.

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